CHIPDESIGN – FROM THEORY TO REAL WORLD

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Overview

- Introduction
- Seminar Description
- The Project
  - Design Concept
  - Project Phases
  - ASIC Manufacturing and Testing
- Evaluation
- Conclusions

Introduction

- University electrical engineering lectures
  - Computer architecture
  - ASIC design
  - Fundamentals of Microelectronic

- Practical training at universities
  - HDL digital design courses limited to FPGA-examples
  - High expenses and experience for EDA-tools required
  - Design issues not included in small projects
- *How to provide a suitable solution?*

ChipDesign Seminar

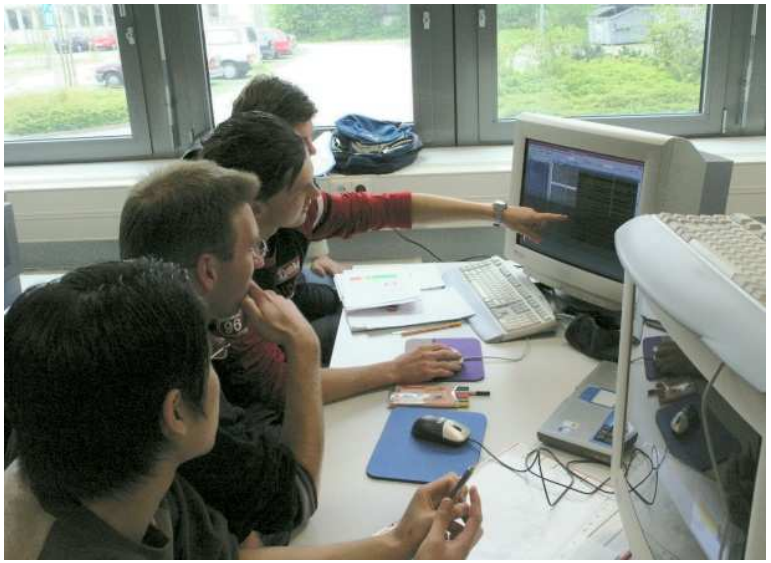
- Project-oriented ASIC design seminar
  - 1999-2002 : Least Cost Router
  - 2003-Today : 8-bit RISC Microcontroller
- Motivation: “From theory to real world”
- Focus
  - Practical knowledge
  - Teamwork experience
- Goal
  - Chip manufacturing

Seminar Description: General

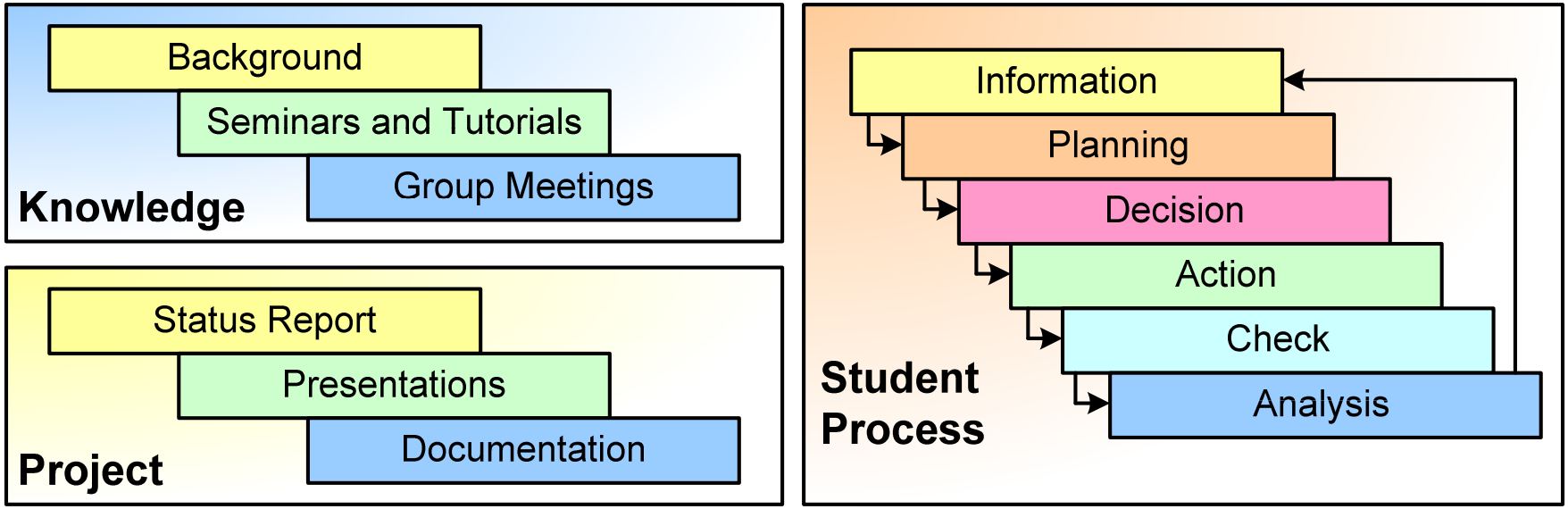
- Extend theorical study by practical aspects
- Duration: 15 week
- ~24 Students
  - Electrical engineering and computer science
  - 3rd - 5th year with bachelor or compatible degree
- Supervision
  - Guaranteed by members of the research staff (tutors)
- Equipment provided by the university
  - Workstations, EDA tools, communication platform,…

Seminar Description: Focus

- Technical skills
  - Design of hardware architectures
  - Hardware description language (verilog)
  - Verification strategies
  - Fundamentals of integrated circuit: Backend
- Social skills
  - Team work (4 students)
  - Responsible for a subtask of the overall project
  - Status meetings and presentations

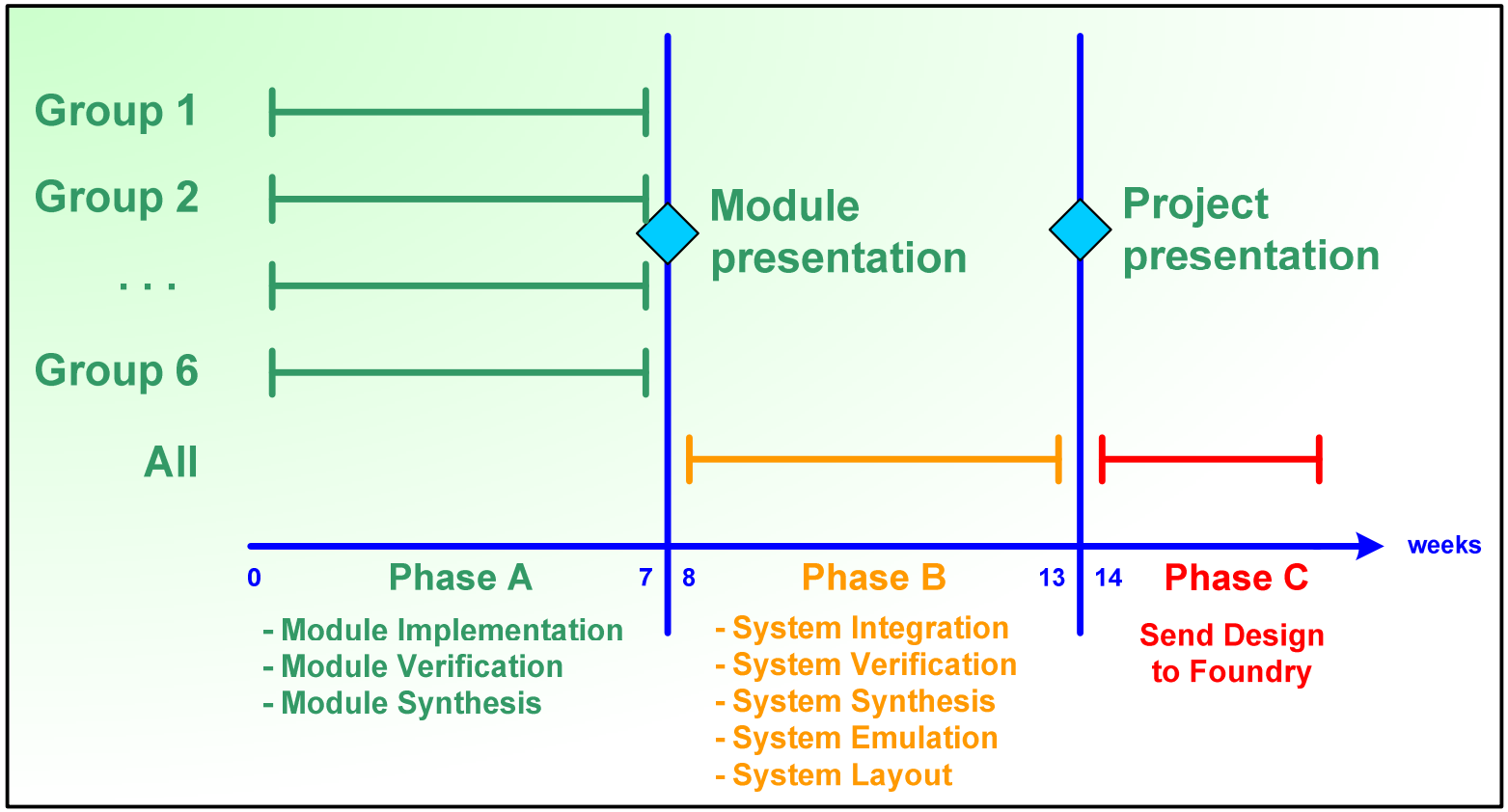


Seminar Description: Learning Approach



- Self-regulated learning
- Knowledge, Student Process and Project
- One group (max.4 students), one tutor, one task

Course Description: Scheduling



- Specific tutorials synchronized with design process
- Status meeting every week

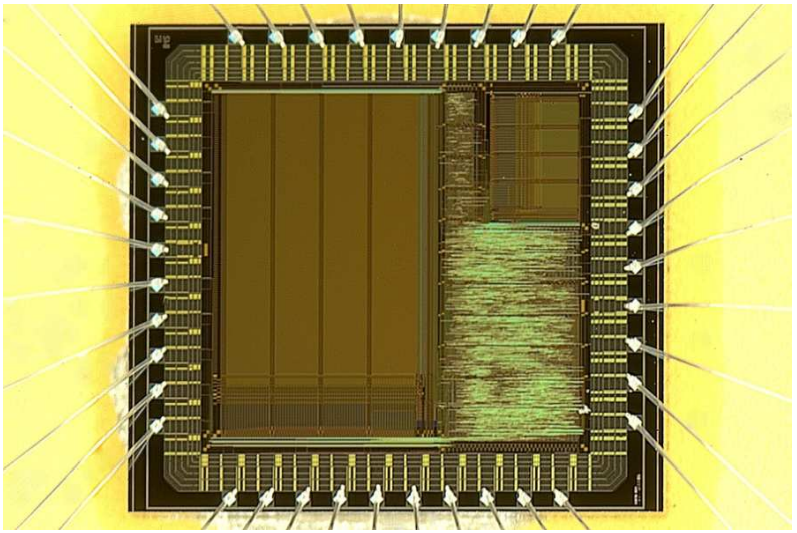
The Project : LCR Design Concept

- Least Cost Router
  - Topic from 1999 to 2002
  - Controller for choosing the cheapest telephone provider
  - Modules:
    - keyboard interface
    - display controller
    - synthesizer for a loudspeaker
    - central control unit

- Problems:
  - Dedicated hardware with limited functionality
  - FSM-based modules with strong dependencies

The Project: *IMS-micro* Design Concept

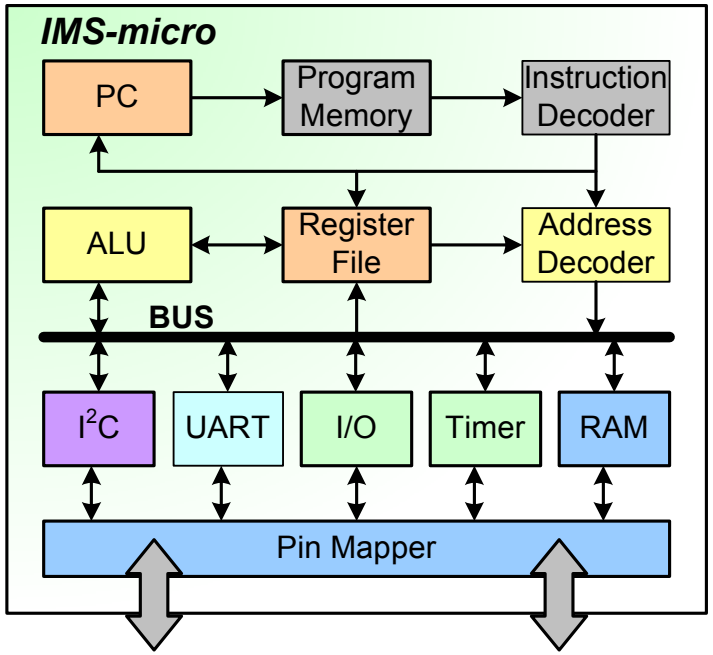
- 8-bit RISC microcontroller
  - Introduced in 2003
  - Programmable hardware design
  - ATMEL AVR 90S8515 instruction set compatible



- Advantages:
  - Education on system level aspects, e.g. computer architecture and low-level software programming
  - Sophisticated modules with fewer dependencies

The Project: Phase A (W0 – W7)

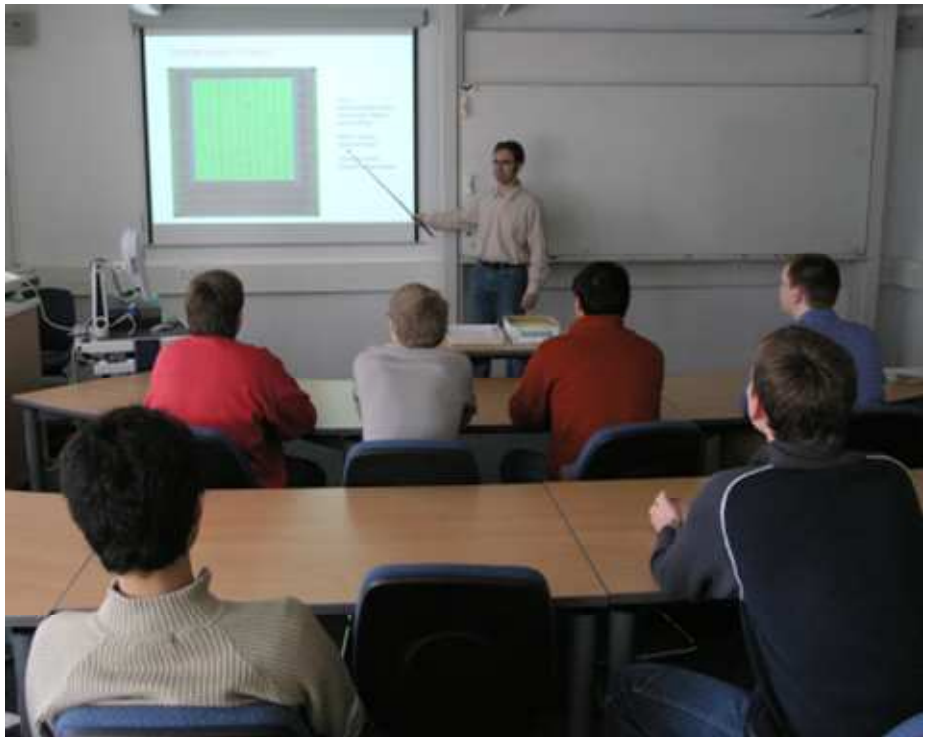
- Module Implementation
  - *Instruction Decoder (given)*
  - Group 1. I2C interface
  - Group 2. SRAM Controller and Pin Mapper
  - Group 3. UART Controller
  - Group 4. Timer and I/0 Ports
  - Group 5. Register File and PC Unit
  - Group 6. ALU and Address Decoder



- Tutorials
  - W1 – Verilog-HDL tutorial
  - W2 – Writing test-benches. Functional verification
  - W3 – Logic Synthesis tutorial

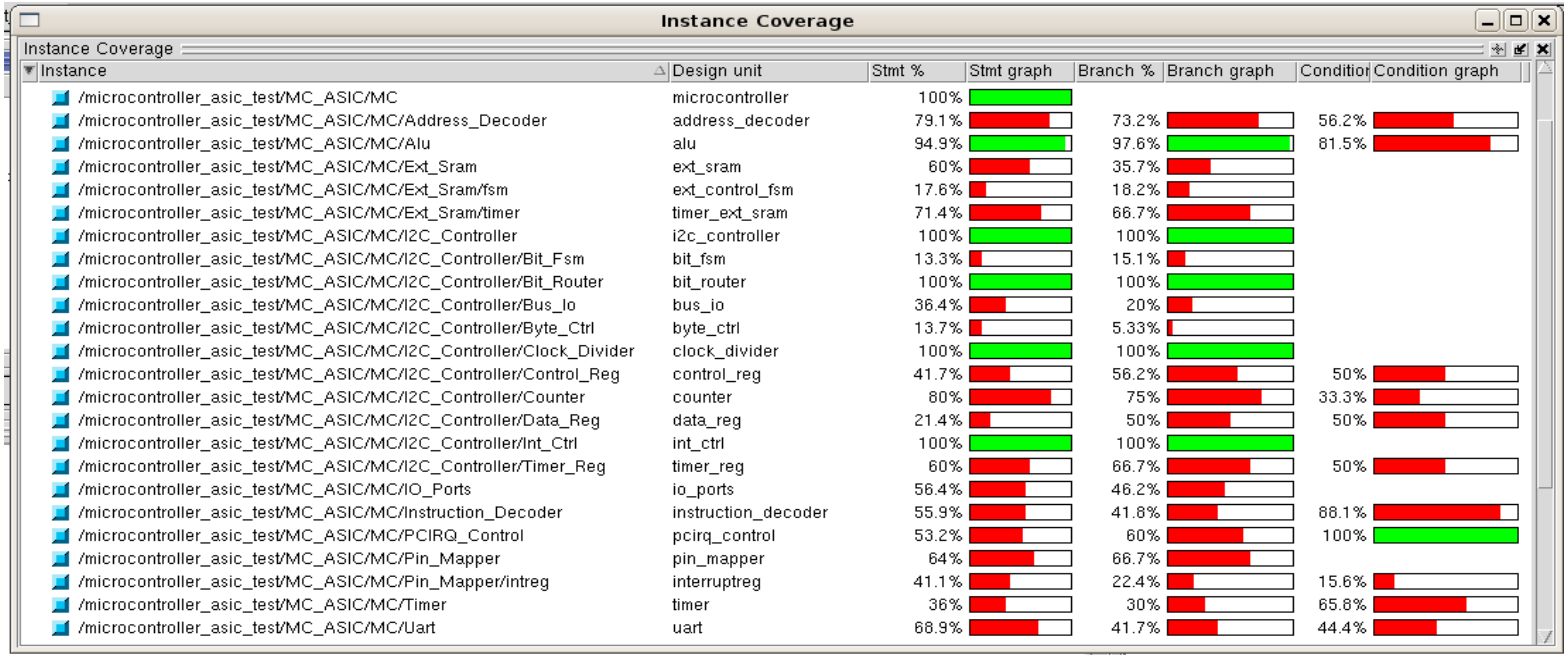
The Project: Phase B (W8 – W13)

- Top-level design
  - Sub-module integration
  - Synthesis
  - Backend
- Top-level verification
  - Simulation environment
  - Assembler programs
  - In-circuit emulation
- Technical documentation
- Social skills: Student communication



The Project: Phase C (W14)

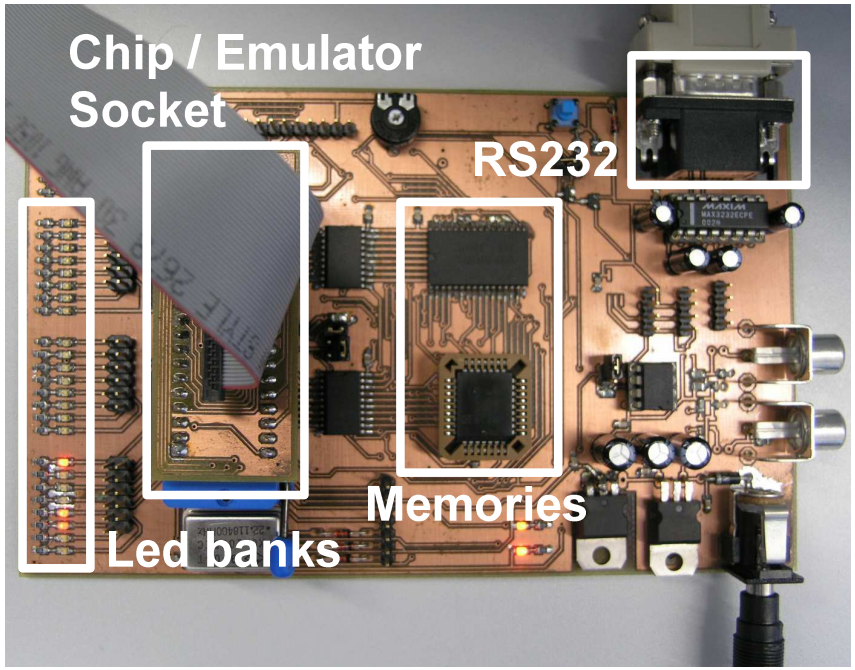
- Extended top-level verification
  - Code coverage (ModelSim)
  - Functional coverage (Automatic test programs)
- Critical path and architecture optimizations



Instance	Design unit	Stmt %	Stmt graph	Branch %	Branch graph	Condition	Condition graph
/microcontroller_asic_test/MC_ASIC/MC	microcontroller	100%					
/microcontroller_asic_test/MC_ASIC/MC/Address_Decoder	address_decoder	79.1%		73.2%		56.2%	
/microcontroller_asic_test/MC_ASIC/MC/Alu	alu	94.9%		97.6%		81.5%	
/microcontroller_asic_test/MC_ASIC/MC/Ext_Sram	ext_sram	60%		35.7%			
/microcontroller_asic_test/MC_ASIC/MC/Ext_Sram/fsm	ext_control_fsm	17.6%		18.2%			
/microcontroller_asic_test/MC_ASIC/MC/Ext_Sram/timer	timer_ext_sram	71.4%		66.7%			
/microcontroller_asic_test/MC_ASIC/MC/I2C_Controller	i2c_controller	100%		100%			
/microcontroller_asic_test/MC_ASIC/MC/I2C_Controller/Bit_Fsm	bit_fsm	13.3%		15.1%			
/microcontroller_asic_test/MC_ASIC/MC/I2C_Controller/Bit_Router	bit_router	100%		100%			
/microcontroller_asic_test/MC_ASIC/MC/I2C_Controller/Bus_Io	bus_io	36.4%		20%			
/microcontroller_asic_test/MC_ASIC/MC/I2C_Controller/Byte_Ctrl	byte_ctrl	13.7%		5.33%			
/microcontroller_asic_test/MC_ASIC/MC/I2C_Controller/Clock_Divider	clock_divider	100%		100%			
/microcontroller_asic_test/MC_ASIC/MC/I2C_Controller/Control_Reg	control_reg	41.7%		56.2%		50%	
/microcontroller_asic_test/MC_ASIC/MC/I2C_Controller/Counter	counter	80%		75%		33.3%	
/microcontroller_asic_test/MC_ASIC/MC/I2C_Controller/Data_Reg	data_reg	21.4%		50%		50%	
/microcontroller_asic_test/MC_ASIC/MC/I2C_Controller/Int_Ctrl	int_ctrl	100%		100%			
/microcontroller_asic_test/MC_ASIC/MC/I2C_Controller/Timer_Reg	timer_reg	60%		66.7%		50%	
/microcontroller_asic_test/MC_ASIC/MC/IO_Ports	io_ports	56.4%		46.2%			
/microcontroller_asic_test/MC_ASIC/MC/Instruction_Decoder	instruction_decoder	55.9%		41.8%		88.1%	
/microcontroller_asic_test/MC_ASIC/MC/PCIRQ_Control	pcirq_control	53.2%		60%		100%	
/microcontroller_asic_test/MC_ASIC/MC/Pin_Mapper	pin_mapper	64%		66.7%			
/microcontroller_asic_test/MC_ASIC/MC/Pin_Mapper/intreg	interruptreg	41.1%		22.4%		15.6%	
/microcontroller_asic_test/MC_ASIC/MC/Timer	timer	36%		30%		65.8%	
/microcontroller_asic_test/MC_ASIC/MC/Uart	uart	68.9%		41.7%		44.4%	

The Project: After the Seminar

- ASIC manufacturing
  - 2003, 2005 and 2006
  - Europractice / Austriamicrosystems AG
  - 0.35 µm CMOS
  - One chip per student



- Testing
  - *IMS-micro* evaluation board
  - Maximum running frequency: 60 MHz (2006)

Evaluation (I)

- Seminar scheduling concept
  - Synchronized with the *IMS-micro* design
  - Tutorial-based
- Supervision concept
  - One tutor per student group
  - Status meetings
- Student prerequisite
  - Pre-selection of participants by written exams
  - Examination results used to divide students into groups

Evaluation (II)

- *IMS-micro* vs. *LCR*
  - *LCR*
    - ✗ dedicated hardware with limited functionality
    - ✓ clearly structured modules with similar complexity
    - ✗ only FSM-based modules with strong dependencies
  - *IMS-micro*
    - ✓ programmable hardware design
    - ✓ more sophisticated design with fewer dependencies
    - ✓ knowledge of the whole architecture required
    - ✓ higher acceptance due to a practical design
- *IMS-micro* is more suited to teach students all aspects of the design process

Conclusions

- Project-oriented ASIC design course
  - Tutorials and practical work separated
  - Whole integrated circuit design flow
  - Improve social skills by giving responsibilities
- Pros vs. cons of *ChipDesign*
  - ✓ Programmable hardware design
  - ✓ System level aspects
  - ✗ Elevated cost (equipments, EDA-tools, tutors,…)
- *After the project, students are ready to design integrated circuits of higher complexity*