#### Didactic Architectures and Simulator for Network Processor Learning

 Henrique Cota de Freitas<sup>1</sup>,
 Carlos Augusto P. S. Martins<sup>2</sup>

 Postgraduate Program in Electrical Engineering

 Pontifical Catholic University of Minas Gerais, Brazil

 <u>cota@pucminas.br<sup>1</sup></u>,

 <u>capsm@pucminas.br<sup>2</sup></u>

 <u>http://www.inf.pucminas.br/projetos/pad-r/r2np.html</u>

# Outline

Introduction and context Objectives and motivations Network Processors overview RNP project RCNP architecture R2NP architecture NPSIM (Network Processor Simulator) Using RNP project to learning NP Commercial architetures of NP Experimental results using NPSIM Conclusions Future works

#### **Introduction and Context**

History GPP's, ASIC's, ASIP's and SoC's Network equipments VHDL and FPGA's Reconfigurable Computing RNP project Didactic architectures and simulator

## **Objectives and motivations**

To present didactic models of Network Processor architectures and a simulator to aid students to learn simple Network Processor architecture concepts.

 to present a *simple way* to learn the main features of Network Processors using didactic architecture models and a simulation tool.
 (nothing related with Network Processors was discovered)

#### **Network Processors Overview**



♦ To analyze and classify the contents of head fields of a packet; ♦ To find in tables association rules related to head fields; To solve the destination path or QoS requirements; ♦ If necessary, to modify the packet (type of service or Diffserv, for example).

# **RNP Project**

- Reconfigurable CISC Network Processor;
- Network Processor Simulator;
- Reconfigurable RISC Network Processor;
- Performance analytical model for the
  - ISA.

#### **RCNP** Architecture



#### **R2NP** Architecture



# NPSIM (Network Processor Simulator)

| <u>File Run Print About H</u> elp  |   |                            |  |  |  |  |   |  |                                |
|--|---|----------------------------|--|--|--|--|---|--|--------------------------------|
| Man 15 MButas 2  |   |                            | 1  |  |  |  |   |  |                                |
| nonnon 43 A Registers  |   | Assembler Permanent Putter |  |  |  |  |   |  |                                |
|  |   |                            | remporary burrers   input Pa   | <u> </u>   |  |  |   |  |                                |
| 000002 00 A 100  |   | LDI D,03                   | _  |  |  |  |   |  |                                |
|  |   | PUT<br>SUI B.00            |  |  |  |  |   |  |                                |
| 000005 03 C 00 D 03 E  |   | JZ 000000                  |  |  |  |  |   |  |                                |
| <u>оооооб FC</u> F JUU G JUU H J   | 6 = 0 0 6   | LDI B,00<br>LDI C,01       |  |  |  |  |   |  |                                |
| 000008 00 PC 00000F  | Control Word  | ENT BC                     |  |  |  |  |   |  |                                |
| 000009 B3  |   | MOV E,A                    |  |  |  |  |   |  |                                |
|  | instruction Heg. [34 Carry [9   | JZ F<br>ANI A,01           |  |  |  |  |   |  |                                |
| 000000 00 Address Register 00000   | 000000 Magnitude Reg. 100   | JMZ 000029                 |  |  |  |  |   |  |                                |
| 000000E 00 Main Buffers - 1/0 P  | rts and Internal Crossbar   | JMZ 000025                 |  |  |  |  |   |  |                                |
| 00000F 98 PUT ENT  | RC SEC SEL SAL  | LDI B,03<br>SEC            |  |  |  |  |   |  |                                |
| 000011 E9 PUT B ENT BC   |   | JMP F                      |  |  | · · · · · · · · · · · · · · · · · · ·  |  |   |  |                                |
| 000012 50  | FCX1  | SEC                        |  |  |  |  |   |  |                                |
| 000013 75 00 00 00   | 00 00 00 00   | JMP F<br>LDLB 01           |  | IL Simulation To   | ol of Network Processor  |  |   | 1 1  |                                |
| 000015 29 B1 B2 B3   | B4 B5 B6 B7 B8  | SEC                        |  | <u>File Bun Print</u>  | <u>A</u> bout <u>H</u> elp   |  |   |  |                                |
| 000010 01  | -SET C.DE   | JMPF                       |  | and the second   |  |  |   |  |                                |
|  |   |                            |  | 71 ·   |  |  |   |  |                                |
| 000018 01<br>000017 B4<br>00000 0000 0000  |   | T                          | F  | Mem 16 MBy   | Registers  |  | Bauman and Buffer   |  | put Packets                    |
| 000017         B4         00000         00000         00000           000018         00         B1         B2         B3   | 0000 0000 0000 0000 0000<br>B4 B5 B6 B7 B8                                | R Ce finen                 | M New Save   | Mem 16 MBy<br>000000 A3<br>000001 00   |  | Decimal  | 1 Permanent Buffer  | rs Temporary Buffers In  | nput Packets                   |
| 000018         01           000017         B4           000018         00           000019         00           B1         B2           000014         23           Fast Access Buttons  | 0000 0000 0000 0000 0000<br>B4 B5 B6 B7 B8                                | C Open                     | E New Save   | Mem 16 MBy<br>000000 A3<br>000001 00<br>000002 00  | Hexadecimal  | Decimal  | 1 Permanent Buffer  | rs Temporary Buffers In<br>Packet Edition Boy  | nput Packets<br><b>x</b>       |
| 000017         B4         Co[co         Co   | 0000 0000 0000 0000 0000<br>B4 B5 B6 B7 B8                                | Initial Adress:            | ∑<br>New Save<br>00 ✓ Byte Assembly  | 4 Mem 16 MBy<br>000000 A3<br>000001 00<br>000002 00<br>000003 06<br>000003 9C  | Registers<br>Hexadecimal   | = 0<br>= 0   | 1 Permanent Buffer  | rs Temporary Buffers In<br>Packet Edition Box  | nput Packets<br><b>x</b>       |
| 000015         01           000017         B4           000019         00           000012         02           000012         02           000010         B1           B2         B3           000012         02           000010         B2  | 0000 0000 0000 0000 0000<br>B4 B5 B6 B7 B8                                | T C Open                   | ▶       ▶    < | Mem.         16 MBy           000000         A3           000001         00           000002         00           000003         06           000004         9C           000005         03  | Hexadecimal           00           8           00           00           00  | Decimal     = 0     = 0     3 0  | 1 Permanent Buffer<br>V/07/143<br>NPSIM: Network<br>Workshop on Nei   | rs Temporary Buffers In<br>Packet Edition Boy<br>Processor Simulator<br>twork Processor  | nput Packets<br><b>x</b>       |
| 000015         01           000017         84           000018         00           000018         00           000018         00           000014         23           000018         02           Fast Access Buttons           000016         02           Image: State Stat  | 0000 0000 0000 0000 0000<br>B4 B5 B6 B7 B8                                | T C Open                   | New Save   | Mem 16 MBy           000000 A3           000001 00           000002 00           000002 00           000002 00           000002 00           000002 00           000005 03           000005 FC           000007 14   | Heighters         Hexadecimal           #         00         B         B         C         C         D         C         C         D         F         C         C         D         C         C         D         C         C         D         C         C         D         C         C         D         C         C         D         C         C         D         C         C         D         C         D         C         D         C         D         C         D         C         D         C         D         C         D         C         D         C         D         C         D         C         D         C         D         C         D         C         D         C         D         D         C         D         D         C         D   | Decimal<br>= 0<br>= 0<br>= 0 3 0<br>= 0 0 6  | 1 Permanent Buffer<br>X/07/143<br>NPSIM: Network<br>Workshop on Ne<br>Pontifical Catholic   | rs Temporary Buffers In<br>Packet Edition Bos<br>Processor Simulator<br>stwork Processor<br>c University of Minas Gerai  | nput Packets<br><b>x</b><br>is |
| 000015         01           000017         B4           000018         00           000018         00           000014         23           000012         02           000012         02           000012         02           000012         02           000012         02           000012         02           000012         02           000012         02           000012         02           000013         03  | 0000 0000 0000 0000 0000<br>B4 B5 B6 B7 B8                                | Initial Adress: 00000      | ∑<br>New Save<br>O <b>✓ Byte</b> Assembly  | Mem 16 MBy           000000 A3           000000 00           000000 00           000000 00           000000 00           000000 00           000000 00           000000 00           000000 00           000000 00           000000 00           000000 FC           000000 1A           000000 FC           000000 1A           000000 FC           000000 0A   | Heighters         Hexadecimal           #         00         Hexadecimal           #         00         D         D           C         00         D         D         E           F         00         G         D         Hexadecimal           PC         00         D         D         E         D           PC         00         D         D         E         D         D  | Desimal           =         0           =         0           =         0           =         0           0         0           6         6           ontrol Word  | 1 Permanent Buffer<br>1/07/143<br>NPSIM: Network<br>Workshop on Net<br>Pontifical Catholic  | rs Temporary Buffers In<br>Packet Edition Box<br>Processor Simulator<br>stwork Processor<br>University of Minas Gerai  | nput Packets<br><b>x</b><br>is |
| 000015         01           000017         B4           000018         00           000018         00           000014         23           000018         02           000018         02           000018         02           000018         02           000018         02           Fast Access Buttons           000010         02           000018         02           000018         02           000018         02           000018         02           000018         02           000018         02           000018         02           000018         02           000018         02           000018         02           000018         02           000018         02           000010         02           000018         02           000018         02           000018         02           000018         02           000018         02           000018         02           000018         02           02   | 0000 0000 0000 0000 0000 0000<br>B4 B5 B6 B7 B8<br>P Step II Reset        | Initial Adress: 00000      | ∑<br>New. Save<br>O ✓ Byte Assembly  | Mem 16 MBy           000000 A3           000001 00           000002 00           000002 00           000002 00           000002 00           000005 03           000005 FC           000007 1A           0000008 00           000009 B3           000009 B3  | tes<br>Registers<br>Hexadecimal<br>00<br>8 00<br>C 00 D 03 E 00<br>F 00 G 00 H 06<br>PC00000F ₽₽ C   | Decimal     = 0     = 0     = 0     = 0     3     0     = 0     0     6     ortrol Word  | 1 Permanent Buffer<br>V/07/143<br>NPSIM: Network<br>Workshop on Ne<br>Pprintical Catholic   | rs Temporary Buffers In<br>Packet Edition Box<br>Processor Simulator<br>stwork Processor<br>University of Minas Gerai  | nput Packets<br><b>x</b><br>is |
| 000013         01           000013         01           000018         00           000010         00           000010         00           000010         00           000010         00           000010         00           000010         00           000010<  | 0000 0000 0000 0000 0000<br>B4 B5 B6 B7 B8<br>P Step II Reset             | Initial Adress: 00000      | ₽<br>New Sove<br>0 ✔ Byte Assembly   | Mem 16 MBy           000000 A3           000001 00           000002 00           000002 00           000002 00           000002 00           000005 03           000005 FC           000007 1A           000008 03           000008 03           000008 00           000008 00           000008 00   | tes<br>Registers<br>Hexadecimal<br>00<br>8 00<br>C 00 D 03 E 00<br>F 00 G 00 H 06<br>PC 000000F ₽₽ C.<br>Status Register 00000000  | Decimal           =         0           =         0           =         0           =         0           0         0           6         0           ontrol Word         Instruction Reg. GA Carry  | 1 Permanent Buffer<br>V/07/143<br>NPSIM: Network<br>Vorkshop on Ne<br>Portifical Catholic   | rs Temporary Buffers In<br>Packet Edition Box<br>Processor Simulator<br>stwork Processor<br>University of Minas Gerai  | nput Packets<br>×              |
| 000013         01           000013         04           000018         00           000019         00           000019         00           000019         00           000019         00           000019         00           000010         00           000010<  | 0000 0000 0000 0000 0000 0000<br>B4 B5 B6 B7 B8                           | Initial Adress: 00000      | ₽<br>New. Sove<br>Sove<br>Byte Assembly  | Mem 16 MBy           000000 A3           000001 00           000002 00           000002 00           000002 00           000002 00           000002 00           000005 03           000005 FC           000005 B3           000005 B3           000005 B3           000006 00           000006 00           000006 00           000006 00   | Heighters         Hexadecimal           00         Hexadecimal           00         D           0000000         D           Address Register         00000000   | Decimal           =         0           =         0           =         0           =         0           0         0           6         0           ontrol Word  | Permanent Buffer     V/07/143     NPSIM: Network     Vorkshop on Ne     Pontifical Catholic     0 00  | rs Temporary Buffers In<br>Packet Edition Box<br>Processor Simulator<br>stwork Processor<br>University of Minas Gerai  | nput Packets<br><b>x</b><br>is |
| 000015         01           000017         84           000018         00           000018         00           000018         00           000018         00           000018         00           000018         00           000018         00           000018         00           000018         00           000011         02           000010         R4  | 0000 0000 0000 0000 0000 0000<br>B4 B5 B6 B7 B8<br><b>D Step D Reset</b>  | Initial Adress: 00000      | ₽<br>New. Sove<br>0 ✔ Byte Assembly  | Mem 16 MBy           000000 A3           000001 00           000002 00           000002 00           000002 00           000002 00           000002 00           000002 00           000005 03           000005 FC           000005 83           000005 83           000005 00           000005 00           000005 00           000005 00           000005 00           000006 00           000007 00           000006 00   | Heighters         Hexadecimal           00         B         00           B         00         C           C         00         D         03           F         00         G         00         H           PC         000000F         C         C         C           Status Register         000000000         O         Address Register         O           Main Buffers         1/0 Ports         1/0 Ports         1/0 Ports  | Decimal           =         0           =         0           =         0           =         0           0         0           =         0           0         0           =         0           0         0           0         0           Instruction Reg.         9A           Carry         00000           Magnitude Reg.         1           and Internal Crossbar   | 1 Permanent Buffer<br>V/07/143<br>NPSIM: Network<br>Vorkshop on Ne<br>Portifical Catholic<br>0<br>00  | rs Temporary Buffers In<br>Packet Edition Box<br>Processor Simulator<br>stwork Processor<br>University of Minas Gerai  | nput Packets<br><b>x</b><br>is |
| 000013         01           000013         00           000013         00           000013         00           000014         20           000015         02           000010         02           000011         02           02 <td>0000 0000 0000 0000 0000<br/>B4 B5 B6 B7 B8<br/><b>D Step II Reset</b></td> <td>Initial Adress: 00000</td> <td>₽<br/>New Sove<br/>0 ✔ Byte Assembly</td> <td>Mem 16 MBy           000000 A3           000001 00           000002 00           000002 00           000002 00           000005 03           000000 FC           000000 00           000000 83           000000 83           000000 83           000000 00           000000 00           000000 00           000000 00           000000 00           000000 00           000000 00           000000 00           000000 00           000000 00           000000 00           000000 00           000000 00           000000 00           000000 00           000000 00           000000 00</td> <td>Heighters         Hexadecimal           00         B         00           B         00         C         00           C         00         D         03         E         00           F         00         G         00         H         06           PC         00000F         F         C         C         Status Register         000000000         C           Address Register         000000000         O         Main Buffers         1/0 Ports         PUT         ENT         BC0</td> <td>Decimal           =         0           =         0           =         0           =         0           =         0           0         0           =         0           0         0           =         0           0         0           0         0           Instruction Reg.         9A           Carry         00000           Magnitude Reg.         1           and Internal Crossbar         SEC           SEC         SEL         SAU</td> <td>1 Permanent Buffer<br/>V/07/143<br/>NPSIM: Network<br/>Vorkshop on Ne<br/>Portifical Catholic<br/>0<br/>00</td> <td>s Temporary Buffers In<br/>Packet Edition Box<br/>Processor Simulator<br/>Itwork Processor<br/>University of Minas Gerai</td> <td>nput Packets<br/>*</td> | 0000 0000 0000 0000 0000<br>B4 B5 B6 B7 B8<br><b>D Step II Reset</b>      | Initial Adress: 00000      | ₽<br>New Sove<br>0 ✔ Byte Assembly   | Mem 16 MBy           000000 A3           000001 00           000002 00           000002 00           000002 00           000005 03           000000 FC           000000 00           000000 83           000000 83           000000 83           000000 00           000000 00           000000 00           000000 00           000000 00           000000 00           000000 00           000000 00           000000 00           000000 00           000000 00           000000 00           000000 00           000000 00           000000 00           000000 00           000000 00   | Heighters         Hexadecimal           00         B         00           B         00         C         00           C         00         D         03         E         00           F         00         G         00         H         06           PC         00000F         F         C         C         Status Register         000000000         C           Address Register         000000000         O         Main Buffers         1/0 Ports         PUT         ENT         BC0  | Decimal           =         0           =         0           =         0           =         0           =         0           0         0           =         0           0         0           =         0           0         0           0         0           Instruction Reg.         9A           Carry         00000           Magnitude Reg.         1           and Internal Crossbar         SEC           SEC         SEL         SAU   | 1 Permanent Buffer<br>V/07/143<br>NPSIM: Network<br>Vorkshop on Ne<br>Portifical Catholic<br>0<br>00  | s Temporary Buffers In<br>Packet Edition Box<br>Processor Simulator<br>Itwork Processor<br>University of Minas Gerai   | nput Packets<br>*              |
| 000013         01           000013         00           000018         00           000018         00           000018         00           000010         00           000010         00           000010         02           000010<  | 0000 0000 0000 0000 0000<br>B4 B5 B6 B7 B8                                | Initial Adress: 00000      | ₽<br>New Sove<br>00 ✔ Byte Assembly  | Mem 16 MBy           000000 A3           000001 00           000002 00           000002 00           000002 00           000005 03           000006 FC           000008 63           000000 00           000000 00           000000 00           000000 00           000000 00           000000 00           000000 00           000000 00           000000 00           000000 00           000000 00           000000 00           000000 00           000000 90           000000 90           000000 90           000000 90           000000 90           000000 90           000000 90           000000 90           000000 90           000000 90           000000 90           000000 90           000000 90           000000 90           000000 90           000000 90   | Hesisters         Hexadecimal           ▲         ↓         ↓           B         ↓         ↓           C         ↓         ↓           PC         ↓         ↓           PC         ↓         ↓           Address         Register         ↓           Address         Register         ↓           PUT         ENT         BAC           PUT         ENT         BAC           PUT         ENT         BCC  | Decimal           =         0           =         0           =         0           =         0           =         0           0         0           =         0           0         0           =         0           0         0           0         6           ontrol Word  | Permanent Buffer     X/07/143     X/07/143     X/05/143     X/05/143     X/05/143     Yokhoo on Ne Pontifical Catholic     O     O  | Temporary Butters In     Packet Edition Bos     Processor Simulator     twork Processor     University of Minas Gerai  | nput Packets<br>*              |
| 000013         01           000013         00           000013         00           000013         00           000013         00           000014         23           000012         02           000010         02           000011         02           000011         02           000011         02           000011         02           000011         02           000011         02           000011         02           000011         02           000011         02           000011         02           000011         02           000011         02           000011         02           000011         02           000011         02           000011         03           000011         04           000011         02           000011         02           000011         02           000011         02           000011         02           011         02           02         02           03  | 0000 0000 0000 0000 0000<br>B4 B5 B6 B7 B8                                | Initial Adress: 00000      | New Save   | Mem 16 MBy           000000 A3           000001 00           000002 01           000002 02           000005 03           000005 03           000007 1A           000008 00           000008 02           000008 03           000007 04           000007 04           000007 04           000007 04           000007 04           000007 04           000007 04           000007 04           000007 04           000007 04           000007 04           000007 05           000007 04           000007 05           000007 04           000007 05           000007 04           000007 05           000007 00           000007 00           000007 01           000007 50   | Ites         Registers           Hexadecimal         Hexadecimal           K         00           B         00           C         00         D           F         00         G         00           F         00         G         00         H           PC         0000F         Image: Color         Color         Color           Status         Register         0000000         Color         Address* Register         Color           Main Buffers         1/0         Ports         Color         For         Ports         Color   | Decimal           =         0           =         0           =         0           =         0           =         0           =         0           0         3           0         6           ontrol Word         Instruction Reg.           Instruction Reg.         9A           O0000         Magnitude Reg.           ond Internal Crossbar         SAI           SEC         SEL           00         0           00         00   | Permanent Buffer     X/07/143     Y/07/143     YosM: Network     YosMin Network      | Temporary Butters In     Packet Edition Bos     Processor Simulator     twork Processor     CUniversity of Minas Gerai   | nput Packets<br>*              |
| 000017         B4           000017         B4           000018         000           000018         00           000018         00           000018         23           000018         00           000018         20           Fast Access Buttons           000018         00           000018         00           P         Run   | 0000 0000 0000 0000 0000 0000<br>B4 B5 B6 B7 B8<br><b>D Step II Reset</b> | Initial Adress: 00000      | New Save   | Mem 16 MBy           000000 A3           000001 00           000002 00           000002 00           000002 00           000002 01           000000 92           000000 92           000000 13           000000 83           000000 83           000000 83           000000 83           000000 83           000000 00           000000 00           000000 00           000000 00           000000 00           000000 00           000000 00           000000 00           000000 98           000000 00           000000 98           000000 11           000000 50           000000 12           000000 50   | Ites         Registers           Hexadecimal         Hexadecimal           K         00           B         00           C         00         D           F         00         G         00           F         00         G         00         H           PC         000000F         Image: Color of the second  | Decimal           =         0           =         0           =         0           =         0           =         0           =         0           0         3           =         0           0         6           ontrol Word         Instruction Reg.           Instruction Reg.         9A           00000         Magnitude Reg.           1         1           000         00   | Permanent Buffer     X/07/143     NPSIM: Network     Vorkhoo on Ne     Pontifical Catholic     0     00     1     00  | Temporary Butters In     Packet Edition Bos     Processor Simulator     twork Processor     Curiversity of Minas Gerai   | nput Packet:<br><b>x</b><br>is |
| 000017         B4           000017         B4           000018         00           000019         00           000019         00           000019         00           000019         00           000019         00           000019         00           000019<  | 0000 0000 0000 0000 0000 0000<br>B4 B5 B6 B7 B8<br><b>D Step II Reset</b> | Initial Adress: 00000      | New Save   | Mem 16 MBy           000000 A3           000001 00           000002 00           000003 06           000005 03           000007 1A           000008 00           000008 00           000009 03           000000 00           000000 00           000006 00           000006 00           000006 00           000006 00           000006 00           000006 00           000006 00           000006 00           000006 00           000000 00   | Hesisters         Hexadecimal           Hexadecimal         Hexadecimal           Hexadecimal         Hexadecimal           C         D0         D           F         D0         D           F         D0         D           PC         D000F         F           C         D         D           F         D         G           PC         D0000F         F           C         C         C           Catus         Register         D000000           Address         Register         D0000000           Main Buffers         1/D Ports           PUTB         ENT BC           D0         D0         D0           PUTB         ENT BC           D0         D0         D0           B1         B2         B3   | Decimal           =         0           =         0           =         0           =         0           =         0           =         0           =         0           =         0           =         0           0         6           ontrol Word  | Permanent Buffer     X/07/143     W75IM: Network     Workboo on Ne     Pontifical Catholic     0 0 0  | s Temporary Butters In<br>Packet Edition Boo<br>Processor Simulator<br>twork Processor<br>c University of Minas Gerai  | nput Packets<br><b>x</b><br>is |
| 000017         B4           000017         B4           000018         00           000018         00           000018         00           000018         20           000018         20           000017         Patholic           000018         20           000017         Patholic           000018         20           000010         Patholic           Patholic         Patholic  | 3000 0000 0000 0000 0000 0000<br>B4 B5 B6 B7 B8<br>I Step II Reset        | Initial Adress: 00000      | ∑<br>New Save<br>0 ✓ Byte Assembly   | Mem 16 MBy           000000 A3           000001 00           000001 00           000002 00           000003 06           000000 42           000000 73           000000 92           000000 71A           000000 83           000000 83           000000 84           000000 84           000000 84           000000 94           000000 94           000000 94           000000 94           000000 94           000000 94           000000 94           000000 94           000000 94           000000 94           000000 94           000000 94           000000 94           000000 94           000000 95           000000 94           000000 95           000000 95           000000 95           000000 95           000000 95           000000 95           000000 95           000000 95           000000 95           000000 95           000000 95           000000 95           000000 95  | Ites         Registers           Hexadecimal         Hexadecimal           Image: Comparison of the second seco | Decimal           =         0           =         0           =         0           =         0           =         0           =         0           =         0           =         0           =         0           0         6           ontrol Word         Instruction Reg.           Instruction Reg.         34           GOUDOO         Magnitude Reg.           and Fitterinal Crossbar         SEC           SEC         SEL           SEL         SEL | Permanent Buffer     X/07/143     Workhoo on Ne     Pontifical Catholic     0 0 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1   | s Temporary Butters In<br>Packet Edition Boo<br>Processor Simulator<br>knock Processor<br>c University of Minas Gerai  | nput Packets<br>x<br>is        |
| 000017         B4           000017         B4           000018         00           000019         00           000018         20           000018         20           000017         Run   | 3000 0000 0000 0000 0000 0000<br>B4 B5 B6 B7 B8<br>IN Step II Reset       | Initial Adress: 00000      | ∑<br>New Save<br>Byte Assembly   | Mem 16 MBy           000000 A3           000000 A3           000000 00           000000 00           000000 00           000000 00           000000 9C           000000 FC           000001 F3           000001 F3           000001 F2           000001 F2           000001 FC           000001 FC   | Ites         Registers           Hexadecimal         Hexadecimal           Image: Comparison of the second seco | Decimal           =         0           =         0           =         0           =         0           =         0           =         0           =         0           =         0           =         0           0         6           ontrol Word         Instruction Reg.           Instruction Reg.         9A           ond         reg.           ond         reg.           on         5EC           SEC         SEL           SEC         SEL        | Permanent Buffer     X/07/143     Workhoo on Ne     Pontifical Catholic     0 0 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1   | ns Temporary Butters In<br>Packet Edition Box<br>Processor Simulator<br>hunderstrong of Minas Gerai<br>c University of Minas Gerai   | nput Packets<br>x<br>is        |
| 000017         B4           000017         B4           000018         00           000018         00           000018         00           000018         00           000018         00           000018         00           000018         00           000018         00           000018         00           000010<  | 0000 0000 0000 0000 0000 0000<br>B4 B5 B6 B7 B8<br>P Step II Reset        | Initial Adress: 00000      | ∑<br>New Save<br>20 ✔Byte Assembly   | Mem 16 MBy           000000 A3<br>000001 00<br>000003 06<br>000003 06<br>000005 FC           000005 FC           000005 FC           000007 IA<br>000008 00           000006 FC           000007 IA<br>000008 00           000006 00           000007 IA<br>000008 00           000006 00           000007 IA<br>000000 00           000000 00           000000 00           000000 11           000001 F3           000001  | Heysters         Hexadecimal           ▲         00           B         00           C         00         D           F         00         00           C         00         00           C         00         00           Address Register         0000000           PUT         ENT BRC           00         00         00           PUT ENT BRC         00           00         00         00           PUT ENT BRC         00         00           B1         B2         B3           B1         B2         B3           B1         B2         B3   | Decimal           =         0           =         0           =         0           =         0           =         0           =         0           =         0           =         0           =         0           0         0           =         0           0         0           Instruction Reg.         9A           Carry         0           ond Internal Crossbar         SAI           00         00         00           SEC         SEL           SAI         00         00           -FCX         00         00         00           4         85         86         87           00         000         000         000         000           4         85         86         87         10   | Permanent Buffer     V07/143     V07/ | n Temporary Buffers In<br>Packet Edition Box<br>Processor Simulator<br>Processor Simulator<br>c University of Minas Gerai  | nput Packets<br>x<br>is<br>S   |
| 000017         04           000017         04           000018         00           000010         00           000010         00           000010         00           000010         00           000010         00           000010         00           000010         00           000010         00           000010         00           000010<  | 0000 0000 0000 0000 0000 0000<br>B4 B5 B6 B7 B8<br>P Step II Reset        | Initial Adress: 00000      | ∑<br>New Save<br>0 ✓ Byte Assembly   | Mem 16 MBy           000000 A3<br>000001 00<br>000003 06<br>000000 9C<br>000005 FC           000005 FC           000005 FC           000007 IA<br>000007 IA           000008 00<br>000000 00           000005 FC           000007 IA           000007 IA           000008 00           000008 00           000009 B3           000000 00           000000 00           000000 9A           000000 9A           000000 00           000000 9A   | Heysters         Hexadecimal           ▲         00           B         00           C         00         D           F         00         D           F         00         D           F         00         H           F         00         H           F         00         H           F         00         H           F         00         C           F         00         C           F         00         C           Calues Register         0000000         G           Address Register         0000000         G           PUT         ENT BAC         F           O0         00         00         00           PUT E         ENT BAC         G           00         00         00         00           B1         B2         B3         B           Fast Access Buttons         F         F   | Decimal           =         0           =         0           =         0           =         0           =         0           =         0           0         0           =         0           0         0           =         0           0         0      <   | Permanent Buffer     V07/143     V07/ | Temporary Buffers In<br>Packet Edition Box<br>Processor Simulator<br>twork Processor<br>cUniversity of Minas Gerai<br>Transport  | is                             |
| 000017         04           000017         04           000018         00           000018         00           000018         00           000018         00           000018         00           000018         00           000018         00           000018         00           000018         00           000018         00           000018         00           000018         00           000018         00           000018         00           000010         00           000018         00           000019         00           000019         00           000010         00           000010         00           000010         00           000010         00           000010         00           000010         00           000010         00           000010         00           000010         00           000010         00           000010         00           000010         00           000010<  | 0000 0000 0000 0000 0000 0000<br>B4 B5 B6 B7 B8<br>Step II Reset          | Initial Adress: 00000      | 2<br>New Save<br>0 V Byte Assembly   | Mem 16 MBy           000000 A3<br>000001 00           000002 00           000003 06           000003 06           000005 70           000007 1A           000008 00           000009 83           000000 00           000000 00           000000 00           000000 00           000000 00           000000 00           000000 94           000000 00           000000 00           000000 00           000000 94           000000 94           000000 94           000000 94           000000 94           000000 94           000000 94           000000 94           000000 94           000000 94           000000 94           000000 94           000000 94           000000 94           000000 94           000000 95           000000 94           000000 95           000000 95           000000 95           000000 95           000000 95           000000 95           000000 95           000000 95 <t< td=""><td>Ites         Registers           Hexadecimal         Hexadecimal           Image: Construction of the second se</td><td>Decimal           =         0           =         0           =         0           =         0           =         0           =         0           =         0           =         0           =         0           0         6           ontrol Word        </td><td>Permanent Buffer     X/07/143     Yokowork     Norkhoo on Ne     Pontifical Catholic     Do     Do     C    C</td><td>In Temporary Butters In Packet Edition Bos<br/>Processor Simulator<br/>Horocessor Simulator<br/>University of Minas Genai<br/>Processor<br/>University of Minas Genai<br/>Processor<br/>Processor<br/>University of Minas Genai<br/>Processor<br/>Processor<br/>Processor<br/>Processor<br/>Processor<br/>Processor<br/>Processor<br/>Processor<br/>Processor<br/>Processor<br/>Processor<br/>Processor<br/>Processor<br/>Processor<br/>Processor<br/>Processor<br/>Processor<br/>Processor<br/>Processor<br/>Processor<br/>Processor<br/>Processor<br/>Processor<br/>Processor<br/>Processor<br/>Processor<br/>Processor<br/>Processor<br/>Processor<br/>Processor<br/>Processor<br/>Processor<br/>Processor<br/>Processor<br/>Processor<br/>Processor<br/>Processor<br/>Processor<br/>Processor<br/>Processor<br/>Processor<br/>Processor<br/>Processor<br/>Processor<br/>Processor<br/>Processor<br/>Processor<br/>Processor<br/>Processor<br/>Processor<br/>Processor<br/>Processor<br/>Processor<br/>Processor<br/>Processor<br/>Processor<br/>Processor<br/>Processor<br/>Processor<br/>Processor<br/>Processor<br/>Processor<br/>Processor<br/>Processor<br/>Processor<br/>Processor<br/>Processor<br/>Processor<br/>Processor<br/>Processor<br/>Processor<br/>Processor<br/>Processor<br/>Processor<br/>Processor<br/>Processor<br/>Processor<br/>Processor<br/>Processor<br/>Processor<br/>Processor<br/>Processor<br/>Processor<br/>Processor<br/>Processor<br/>Processor<br/>Processor<br/>Processor<br/>Processor<br/>Processor<br/>Processor<br/>Processor<br/>Processor<br/>Processor<br/>Processor<br/>Processor<br/>Processor<br/>Processor<br/>Processor<br/>Processor<br/>Processor<br/>Processor<br/>Processor<br/>Processor<br/>Processor<br/>Processor<br/>Processor<br/>Processor<br/>Processor<br/>Processor<br/>Processor<br/>Processor<br/>Processor<br/>Processor<br/>Processor<br/>Processor<br/>Processor<br/>Processor<br/>Processor<br/>Processor<br/>Processor<br/>Processor<br/>Processor<br/>Processor<br/>Processor<br/>Processor<br/>Procesor<br/>Processor<br/>Processor<br/>Processor<br/>Processor<br/>Proce</td><td>sput Packet:</td></t<> | Ites         Registers           Hexadecimal         Hexadecimal           Image: Construction of the second se | Decimal           =         0           =         0           =         0           =         0           =         0           =         0           =         0           =         0           =         0           0         6           ontrol Word  | Permanent Buffer     X/07/143     Yokowork     Norkhoo on Ne     Pontifical Catholic     Do     Do     C    C | In Temporary Butters In Packet Edition Bos<br>Processor Simulator<br>Horocessor Simulator<br>University of Minas Genai<br>Processor<br>University of Minas Genai<br>Processor<br>Processor<br>University of Minas Genai<br>Processor<br>Processor<br>Processor<br>Processor<br>Processor<br>Processor<br>Processor<br>Processor<br>Processor<br>Processor<br>Processor<br>Processor<br>Processor<br>Processor<br>Processor<br>Processor<br>Processor<br>Processor<br>Processor<br>Processor<br>Processor<br>Processor<br>Processor<br>Processor<br>Processor<br>Processor<br>Processor<br>Processor<br>Processor<br>Processor<br>Processor<br>Processor<br>Processor<br>Processor<br>Processor<br>Processor<br>Processor<br>Processor<br>Processor<br>Processor<br>Processor<br>Processor<br>Processor<br>Processor<br>Processor<br>Processor<br>Processor<br>Processor<br>Processor<br>Processor<br>Processor<br>Processor<br>Processor<br>Processor<br>Processor<br>Processor<br>Processor<br>Processor<br>Processor<br>Processor<br>Processor<br>Processor<br>Processor<br>Processor<br>Processor<br>Processor<br>Processor<br>Processor<br>Processor<br>Processor<br>Processor<br>Processor<br>Processor<br>Processor<br>Processor<br>Processor<br>Processor<br>Processor<br>Processor<br>Processor<br>Processor<br>Processor<br>Processor<br>Processor<br>Processor<br>Processor<br>Processor<br>Processor<br>Processor<br>Processor<br>Processor<br>Processor<br>Processor<br>Processor<br>Processor<br>Processor<br>Processor<br>Processor<br>Processor<br>Processor<br>Processor<br>Processor<br>Processor<br>Processor<br>Processor<br>Processor<br>Processor<br>Processor<br>Processor<br>Processor<br>Processor<br>Processor<br>Processor<br>Processor<br>Processor<br>Processor<br>Processor<br>Processor<br>Processor<br>Processor<br>Processor<br>Processor<br>Processor<br>Processor<br>Processor<br>Processor<br>Procesor<br>Processor<br>Processor<br>Processor<br>Processor<br>Proce | sput Packet:                   |

## **Using RNP project to learn NP**



#### **Commercial Architectures of NP**





The R2NP is 4,44 faster than RCNP for hypercube simulation. The R2NP is 3,47 faster than RCNP for unidrectional ring simulation. The R2NP is 2,94 faster than RCNP for balanced tree simulation.

## Conclusions



- Four commercial architectures were presented and related with the reference to show the use of didactic models before the studying of commercial Network Processors.
- The results validated our goals and showed how conceptual models can aid students to understand complex architectures of Network Processors.
- A paper or research with didactic features for NP's, were not found.

## **Future works**

To simulate R2NP with Rconf\_KMT (Reconfigurable Simulation Tool) and VHDL (VHSIC Hardware Description Language),

- to prototype with FPGA (Field Programmable Gate Array),
- to simulate it in a real network system,
- to develop didactic environment to learn Network Processors.

#### Didactic Architectures and Simulator for Network Processor Learning

 Henrique Cota de Freitas<sup>1</sup>,
 Carlos Augusto P. S. Martins<sup>2</sup>

 Postgraduate Program in Electrical Engineering

 Pontifical Catholic University of Minas Gerais, Brazil

 <u>cota@pucminas.br<sup>1</sup></u>,

 <u>capsm@pucminas.br<sup>2</sup></u>

 <u>http://www.inf.pucminas.br/projetos/pad-r/r2np.html</u>