Didactic Architectures and Simulator for Network Processor Learning

Henrique Cota de Freitas[1], Carlos Augusto P. S. Martins[2]

Postgraduate Program in Electrical Engineering

Pontifical Catholic University of Minas Gerais, Brazil

cota@pucminas.br[1], *capsm@pucminas.br*[2]

http://www.inf.pucminas.br/projetos/pad-r/r2np.html

Outline

- Introduction and context
- Objectives and motivations
- Network Processors overview
- RNP project
- RCNP architecture
- R2NP architecture
- NPSIM (Network Processor Simulator)
- Using RNP project to learning NP
- Commercial architetures of NP
- Experimental results using NPSIM
- Conclusions
- Future works

Introduction and Context

- History
  - GPP's, ASIC's, ASIP's and SoC's
- Network equipments
- VHDL and FPGA's
- Reconfigurable Computing
- RNP project
- Didactic architectures and simulator

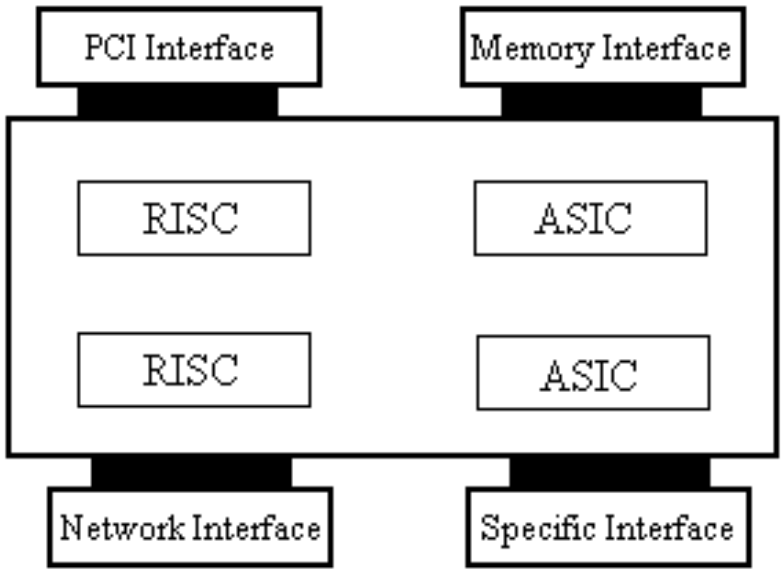
Objectives and motivations

- to present *didactic models of Network Processor architectures and a simulator* to aid students to learn simple Network Processor architecture concepts.

- to present a *simple way* to learn the main features of Network Processors using didactic architecture models and a simulation tool.

  (nothing related with Network Processors was discovered)

Network Processors Overview

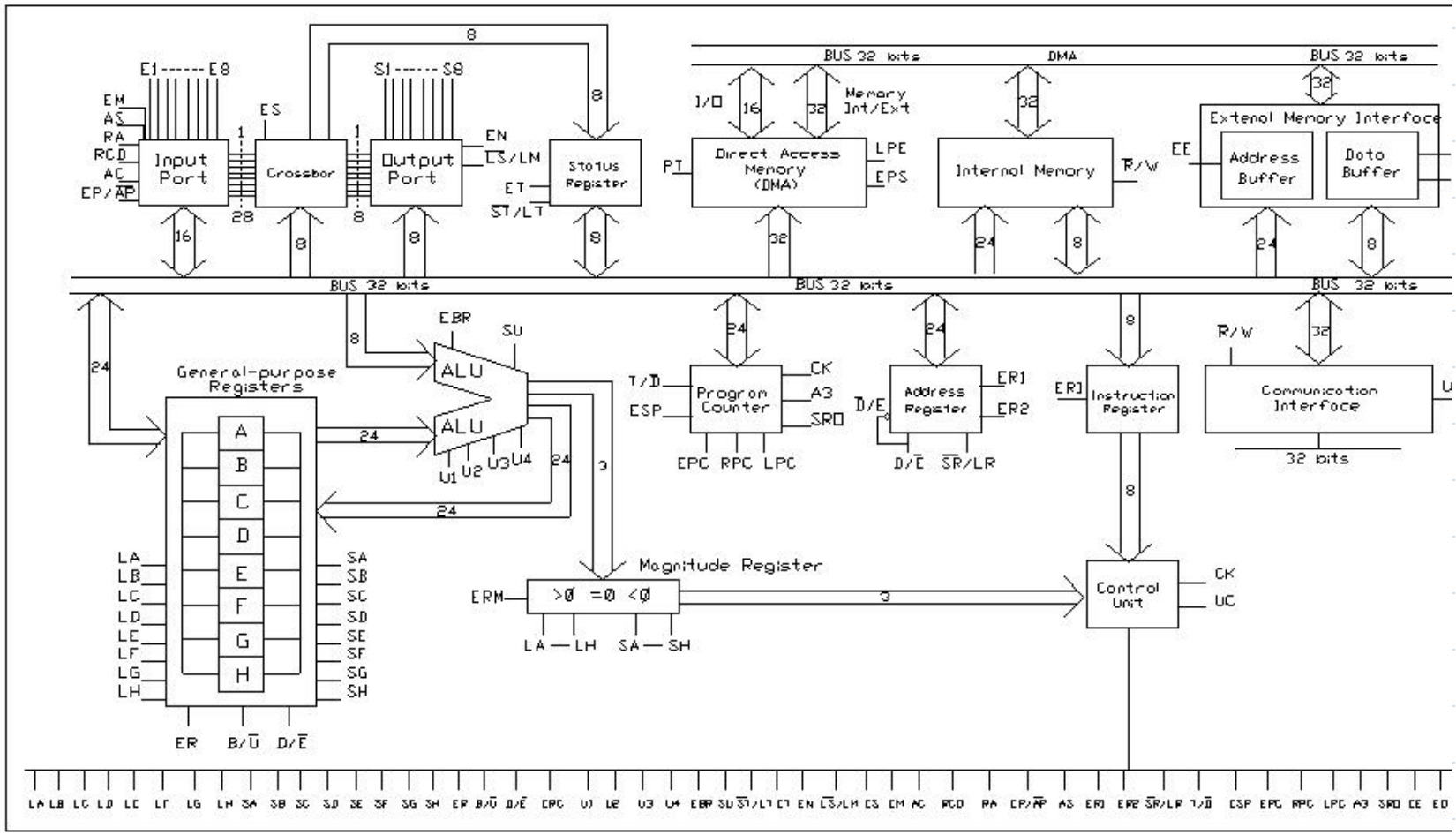


- To analyze and classify the contents of head fields of a packet;
- To find in tables association rules related to head fields;
- To solve the destination path or QoS requirements;
- If necessary, to modify the packet (type of service or Diffserv, for example).

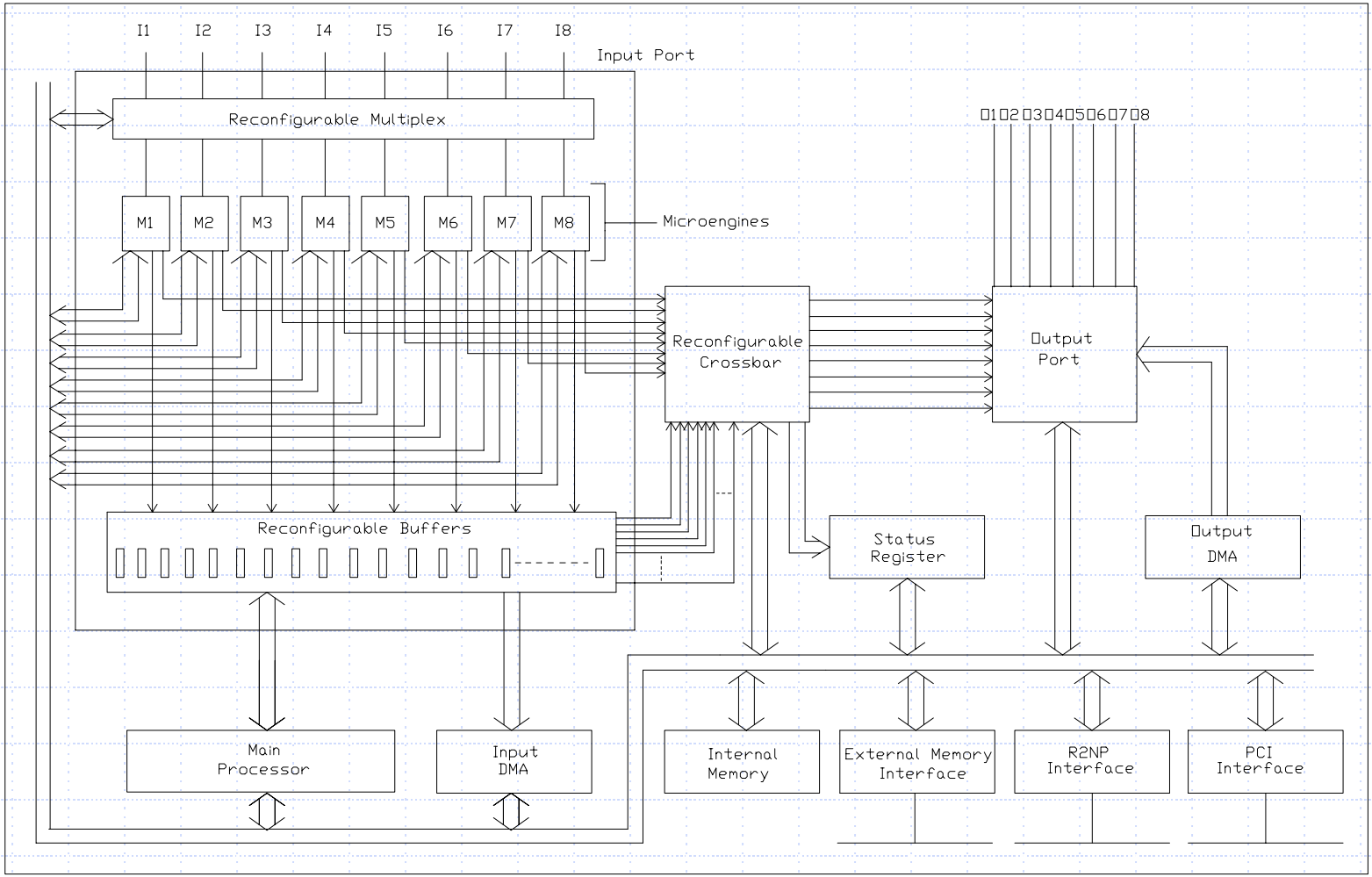
RNP Project

- Reconfigurable CISC Network Processor;
- Network Processor Simulator;
- Reconfigurable RISC Network Processor;
- Performance analytical model for the ISA.

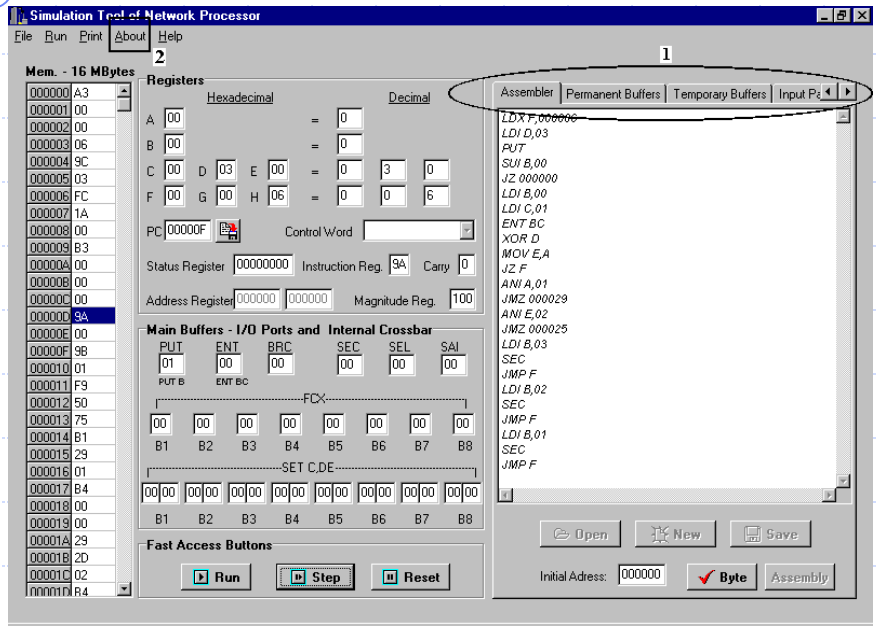
RCNP Architecture

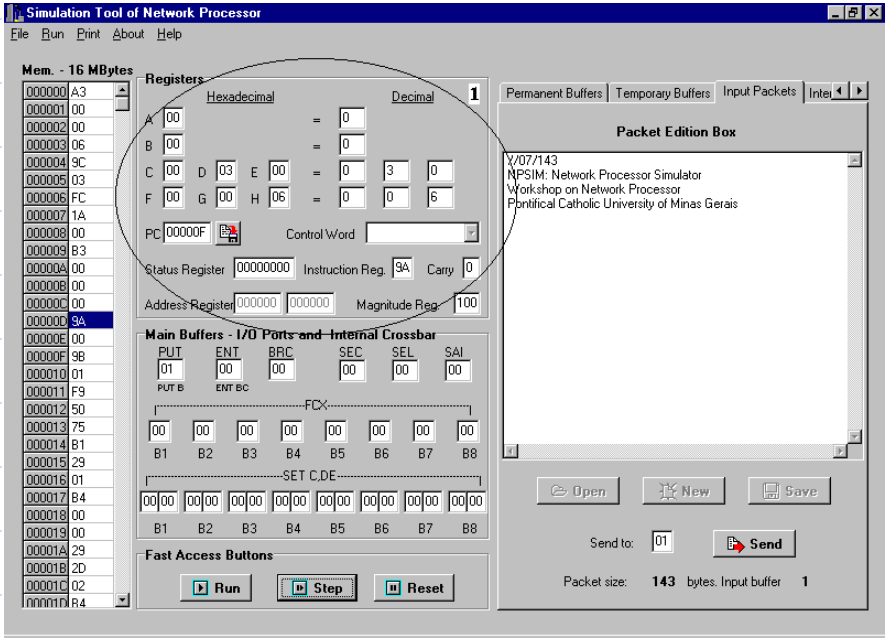


R2NP Architecture

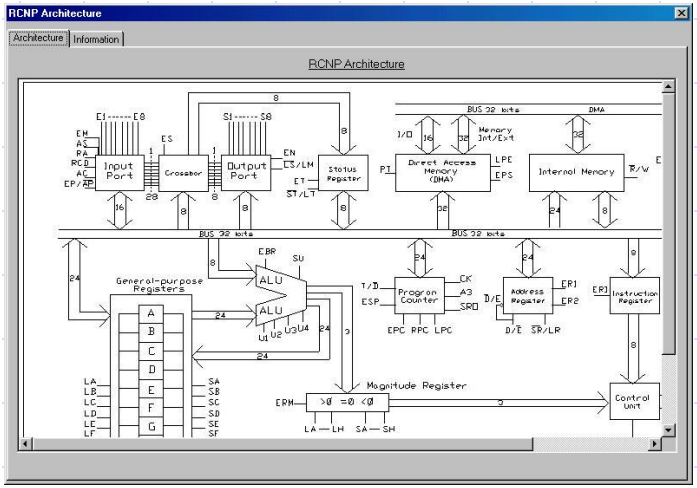


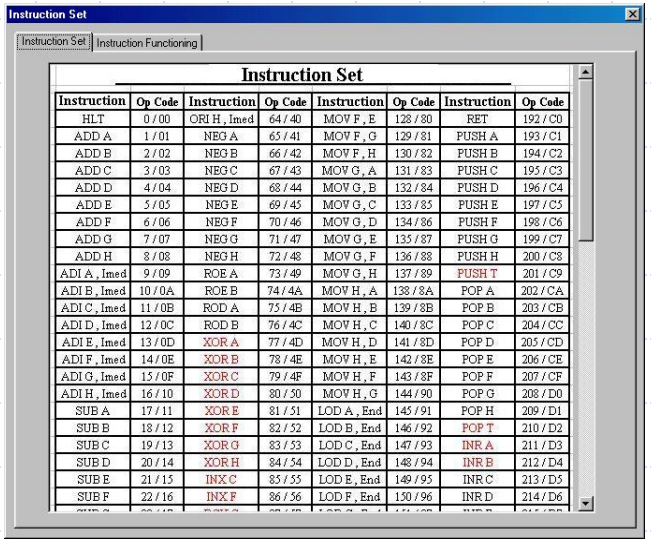
NPSIM (Network Processor Simulator)



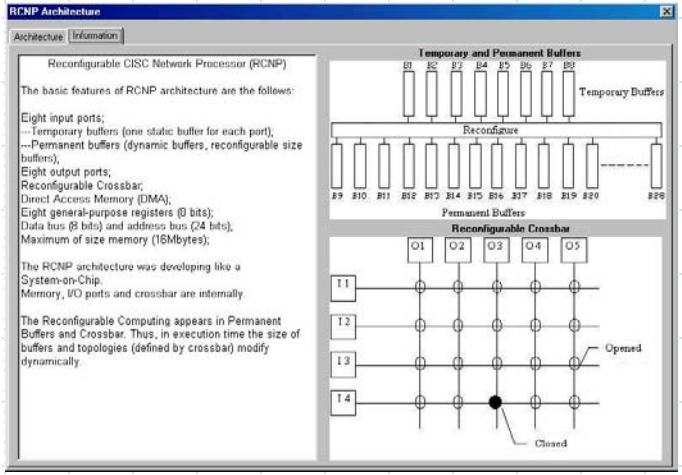


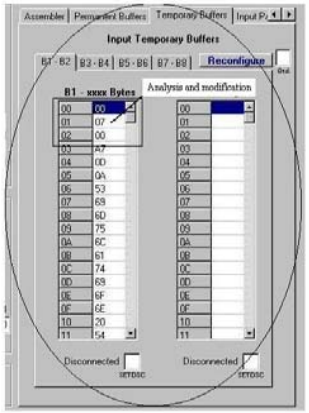
Using RNP project to learn NP

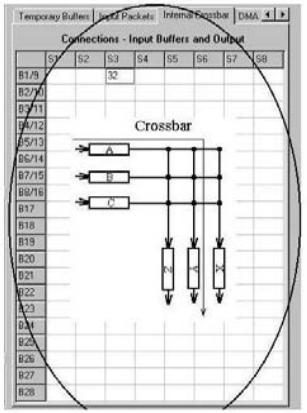




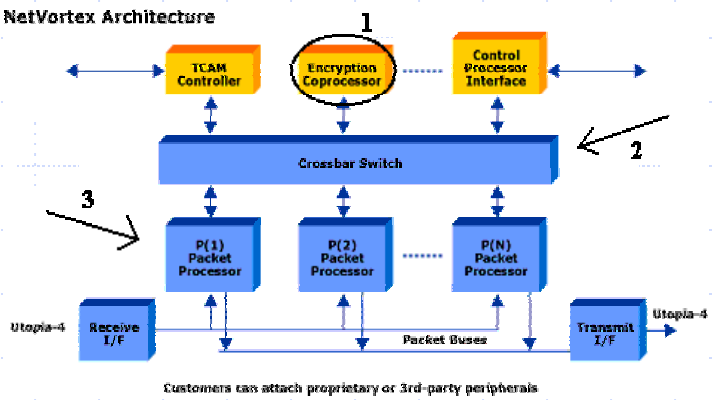
Instruction	Op Code	Instruction	Op Code	Instruction	Op Code	Instruction	Op Code
HLT	0 / 00	ORI H , Imed	64 / 40	MOV F , E	128 / 80	RET	192 / C0
ADD A	1 / 01	NEG A	65 / 41	MOV F , G	129 / 81	PUSH A	193 / C1
ADD B	2 / 02	NEG B	66 / 42	MOV F , H	130 / 82	PUSH B	194 / C2
ADD C	3 / 03	NEG C	67 / 43	MOV G , A	131 / 83	PUSH C	195 / C3
ADD D	4 / 04	NEG D	68 / 44	MOV G , B	132 / 84	PUSH D	196 / C4
ADD E	5 / 05	NEG E	69 / 45	MOV G , C	133 / 85	PUSH E	197 / C5
ADD F	6 / 06	NEG F	70 / 46	MOV G , D	134 / 86	PUSH F	198 / C6
ADD G	7 / 07	NEG G	71 / 47	MOV G , E	135 / 87	PUSH G	199 / C7
ADD H	8 / 08	NEG H	72 / 48	MOV G , F	136 / 88	PUSH H	200 / C8
ADI A , Imed	9 / 09	ROE A	73 / 49	MOV G , H	137 / 89	PUSH T	201 / C9
ADI B , Imed	10 / 0A	ROE B	74 / 4A	MOV H , A	138 / 8A	POP A	202 / CA
ADI C , Imed	11 / 0B	ROD A	75 / 4B	MOV H , B	139 / 8B	POP B	203 / CB
ADI D , Imed	12 / 0C	ROD B	76 / 4C	MOV H , C	140 / 8C	POP C	204 / CC
ADI E , Imed	13 / 0D	XOR A	77 / 4D	MOV H , D	141 / 8D	POP D	205 / CD
ADI F , Imed	14 / 0E	XOR B	78 / 4E	MOV H , E	142 / 8E	POP E	206 / CE
ADI G , Imed	15 / 0F	XOR C	79 / 4F	MOV H , F	143 / 8F	POP F	207 / CF
ADI H , Imed	16 / 10	XOR D	80 / 50	MOV H , G	144 / 90	POP G	208 / D0
SUB A	17 / 11	XOR E	81 / 51	LOD A , End	145 / 91	POP H	209 / D1
SUB B	18 / 12	XOR F	82 / 52	LOD B , End	146 / 92	POP T	210 / D2
SUB C	19 / 13	XOR G	83 / 53	LOD C , End	147 / 93	INR A	211 / D3
SUB D	20 / 14	XOR H	84 / 54	LOD D , End	148 / 94	INR B	212 / D4
SUB E	21 / 15	INX C	85 / 55	LOD E , End	149 / 95	INR C	213 / D5
SUB F	22 / 16	INX F	86 / 56	LOD F , End	150 / 96	INR D	214 / D6

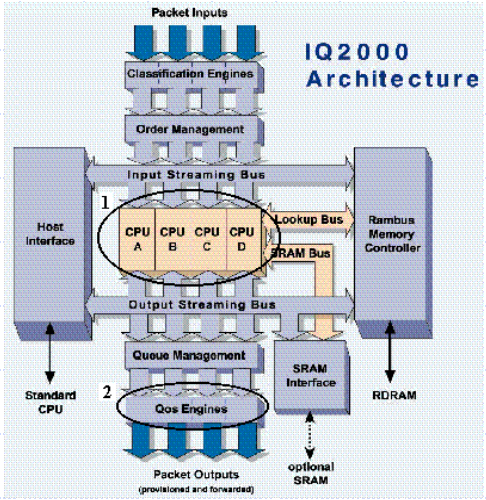


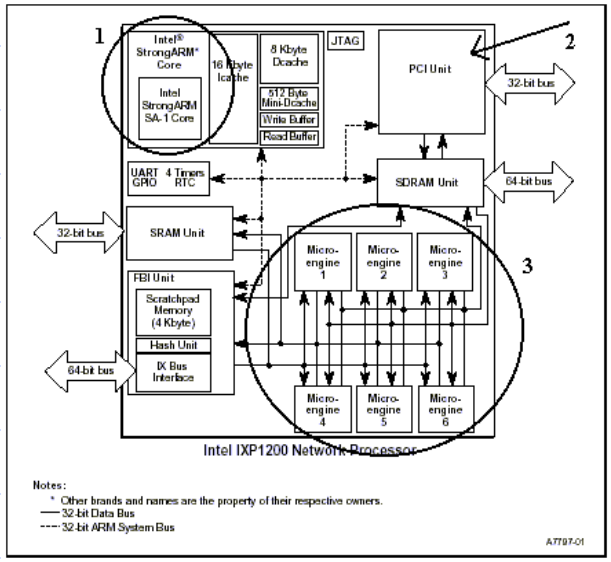


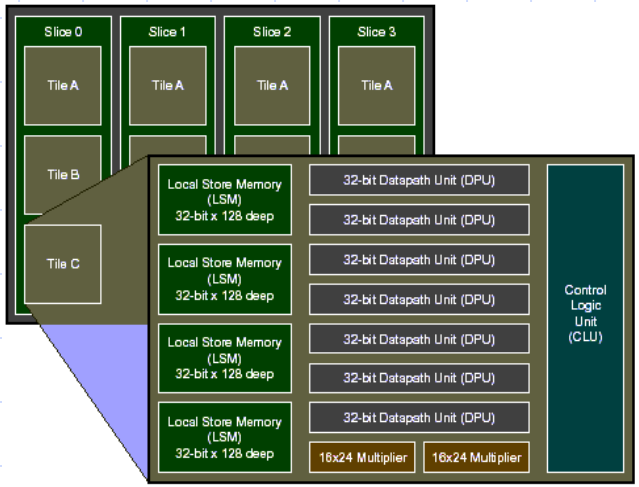


Commercial Architectures of NP

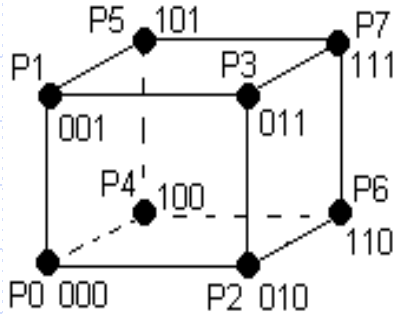




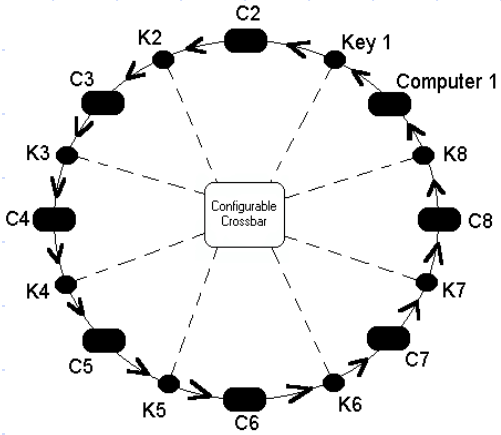




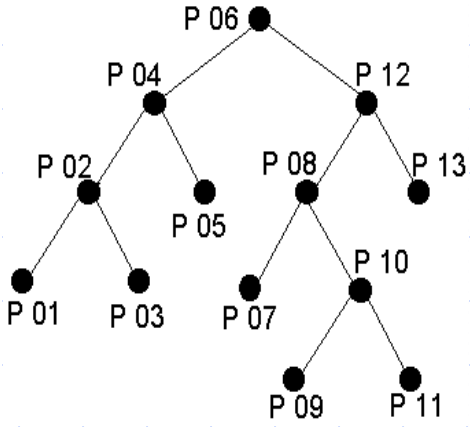
Experimental results using NPSIM



Hypercube Topology



Unidirectional ring Topology



Balanced tree Topology

The R2NP is 4,44 faster than RCNP for hypercube simulation.
The R2NP is 3,47 faster than RCNP for unidirectional ring simulation.
The R2NP is 2,94 faster than RCNP for balanced tree simulation.

Conclusions

- The same features in reference architecture appear in RNP project. Using these didactic proposals it is possible to learn the basic concepts.
- Four commercial architectures were presented and related with the reference to show the use of didactic models before the studying of commercial Network Processors.
- The results validated our goals and showed how conceptual models can aid students to understand complex architectures of Network Processors.
- A paper or research with didactic features for NP's, were not found.

Future works

- To simulate R2NP with Rconf_KMT (Reconfigurable Simulation Tool) and VHDL (VHSIC Hardware Description Language),
- to prototype with FPGA (Field Programmable Gate Array),
- to simulate it in a real network system,
- to develop didactic environment to learn Network Processors.

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